Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): An apparatus comprising:

an input block to apply an input signal to a common input terminal of a sensing block, the input block coupled to apply a first signal to the common input terminal during a first clock phase of a first clock and a second signal during a second clock phase of a second clock; and

a converting block to receive a sensed signal from the sensing block in response to the input signal.

Claim 2 (previously presented): The apparatus of claim 1, wherein the converting block is coupled to provide an output signal based on the sensed signal.

Claim 3 (cancel)

Claim 4 (cancelled)

Claim 5 (currently amended): The apparatus of claim 1, wherein the converting block ~~is configured to~~ comprises an integrator to integrate the sensed signal and provide a first output signal and a second output signal.

Claim 6 (previously presented): The apparatus of claim 5, wherein the converting block is further configured to compare the first output signal and the second output signal and provide an output signal.

Claim 7 (previously presented): The apparatus of claim 6, wherein the converting block is coupled to provide the output signal to the input block.

Claim 8 (currently amended): The apparatus of claim 1, wherein the input block comprises a first input capacitor and a second input capacitor, wherein the input block is coupled to provide a first input signal [[to]] into the converting block through the first input capacitor and a second input signal [[to]] into the converting block through the second input capacitor.

Claim 9 (cancel)

Claim 10 (currently amended): The apparatus of claim 1, further comprising a storage unit to store one or more voltage values to couple ~~apply~~ to a first input capacitor and a second input capacitor of the apparatus.

Claim 11 (currently amended): A method comprising:

providing a first signal to a common input terminal of a sensing block during a first clock phase of a first clock and a second signal to the common input terminal during a second clock phase of a second clock, wherein the first clock phase and the second clock phase have non-overlapping clock cycles;

receiving a sensed signal from the sensing block based on providing the first signal and the second signal; and

providing a signal based on the sensed signal.

Claim 12 (cancel)

Claim 13 (cancel)

Claim 14 (canceled)

Claim 15 (canceled)

Claim 16 (currently amended): The method of claim 11, comprising integrating the sensed signal and providing a first output signal and a second output signal.

Claim 17 (previously presented): The method of claim 16, comprising comparing the first output signal and the second output signal ~~and providing~~ to provide an output signal.

Claim 18 (original): The method of claim 17, comprising providing the first signal and second signal based at least in part on the output signal.

Claims 19-24 (cancel)

Claim 25 (currently amended): A restraint system, comprising:

a sensing circuit to:

apply an input signal to a common input terminal of a sensing block;

receive a sensed signal from the sensing block in response to applying the input signal; and

provide an output signal based at least in part on the sensed signal; ~~and~~

a deployment block to provide an activation signal based at least in part on the output signal from the sensing circuit; and

a control unit to provide a control signal to the deployment block.

Claim 26 (previously presented): The restraint system of claim 25, wherein the deployment block is coupled to provide the activation signal to activate an airbag.

Claim 27 (previously presented): The restraint system of claim 25, wherein the sensing circuit is coupled to be clocked via a plurality of non-overlapping clocks.

Claim 28 (previously presented): The restraint system of claim 25, wherein the sensing circuit is configured to provide a digital signal.

Claim 29 (previously presented): The restraint system of claim 25, wherein the sensing circuit is coupled to provide a signal having a fractional pulse density that is indicative of acceleration.

Claim 30 (original): The restraint system of claim 25, further comprising a storage unit to store one or more voltage values to apply to the sensing circuit.

Claim 31 (new): The apparatus of claim 1, wherein the sensing block comprises a pair of output terminals to provide the sensed signal.

Claim 32 (new): The apparatus of claim 1, wherein the first clock and the second clock are non-overlapping.

Claim 33 (new): The apparatus of claim 10, wherein the voltage values comprise calibration voltages, the calibration voltages to couple to a first input capacitor and a second input capacitor.

Claim 34 (new): The method of claim 11, further comprising directly providing the first signal using a first reference voltage and the second signal using a second reference voltage.

Claim 35 (new): The method of claim 11, further comprising calibrating the sensing block using a first input capacitor and a second input capacitor.

Claim 36 (new): The restraint system of claim 25, wherein the sensing block comprises a pair of output terminals to provide the sensed signal.